Machine Learning-Driven Optimization of Silicon Wafer Thinning for Hardware Security Applications

Eric Mottay[1], Wahib Migan Barkat, [2] Emile Barjou[2], Anthony Bertrand[2], Girolamo Mincuzzi,[2]

1- h-nu, 33130 Begles, France
2- Alphanov, 33400 Talence, France

Corresponding author: eric.mottay@h-nu.net

The reliability of Integrated Circuits is critical, especially in harsh environments where operational failures can occur. High-energy cosmic rays, for example, may induce transient or permanent defects in circuits responsible for vital functions, such as those in spacecraft. As circuits grow more complex, the likelihood of failure increases. To trace the origins of such defects, Failure Analysis often involves techniques like external examination, continuity testing, decapsulation, and Scanning Electron Microscopy paired with Energy Dispersive X-ray Spectroscopy. Decapsulation methods—such as wet chemistry, plasma etching, or laser ablation—must be performed carefully to avoid further damage. In backside Failure Analysis, most of the silicon die must be removed through precise silicon wafer thinning to access the circuitry and locate the failure.

Machine learning offers a promising solution for predicting ablation depth and surface roughness during silicon wafer thinning. However, it requires extensive and time-consuming data acquisition. To address this challenge, we developed an automated acquisition protocol using a confocal profilometer, capturing topographical data from hundreds of ablation images across silicon and steel samples. By applying regression algorithms and Convolutional Neural Networks, we predict ablation depth, surface roughness, and large-scale surface patterns. The model translates parameters such as laser energy and the number of passes into image data for pattern recognition and roughness evaluation. Dual loss functions further enhance prediction accuracy. Results show a strong correlation between predicted and actual values, demonstrating reliable generalization across materials.

Future work will focus on developing real-time diagnostics for dynamic adjustments during the thinning process, further improving precision and efficiency for hardware security evaluations.